# CLAIMS

1. A redundancy address decoder for a memory having at least one bank of memory segmented into a plurality of memory blocks, each memory block having a redundancy plane and having a programmable element block storing programmed addresses that are mapped to redundant memory of the redundancy plane, the redundancy address decoder comprising:

a plurality of redundancy comparison circuitry coupled to a respective one of the programmable element blocks to generate a match signal in response to detecting an address match with one of the programmed addresses; and

redundancy driver select logic coupled to each of the redundancy comparison circuitry to activate a selected one of the redundancy comparison circuitry for comparing a portion of a memory address corresponding to a memory location with the programmed addresses of the respective programmable element blocks, the activation by the redundancy driver based on the memory block in which the memory location is located.

2. The redundancy address decoder of claim 1 wherein the memory address is represented by a plurality of memory address signals and the redundancy comparison circuitry comprises:

a redundancy driver having input address terminals to which the memory address signals are applied, output address terminals at which output address signals are provided, and an activation terminal to which an activation signal from the redundancy driver select logic is applied, the redundancy driver coupling the input address terminals to the output address terminals in response to the activation signal; and

redundancy comparison logic coupled to the respective programmable element block and further coupled to the output address terminals of the redundancy driver to receive the memory address signals for comparison to the programmed addresses of the respective programmable element block.

3. The redundancy address decoder of claim 2 wherein the redundancy driver comprises logic circuitry to block the switching of the logic states of the memory address signals applied to the respective redundancy comparison logic when deactivated and to allow the switching of logic states of the memory address signals applied to the respective redundancy comparison logic when activated.

4. The redundancy address decoder of claim 2 wherein the redundancy driver comprises a plurality of NAND gates, each NAND gate having a first input coupled to the redundancy driver select logic and a second input to a respective one of the input address terminals.

5. The redundancy address decoder of claim 1 wherein the programmable element block comprises a plurality of antifuse elements programmed with column addresses of memory locations mapped to the respective redundancy plane.

6. The redundancy address decoder of claim 1 wherein the redundancy driver select logic comprises a plurality of NOR gates, each NOR gate having a different combination of a selection signal and its complement as input signals, the selection signal indicative of the memory bank in which the memory location is located.

7. The redundancy address decoder of claim 6 wherein the portion of the memory address compared by a selected one of the redundancy comparison circuitry comprises a column address and the selection signal comprises a portion of a row address.

8. A redundancy address decoder for a memory device having a memory array divided into at least one bank of memory, each bank of memory segmented into a plurality of memory blocks having a respective redundancy plane of redundant memory, the redundancy address decoder comprising:

for each redundancy plane in the bank of memory, a programmable element block, redundancy comparison logic coupled to the programmable element block, and a redundancy driver coupled to the redundancy comparison logic, the redundancy driver having input address terminals at which memory address signals corresponding to a memory address are applied and having output address terminals to which the memory address signals are coupled in response to activation of the redundancy driver, the comparison logic comparing the memory address signals from the redundancy driver to redundancy memory addresses stored in the programmable element block and generating a match signal in response to detecting an address match between the memory address signals and a redundancy memory address; and

redundancy driver select logic coupled to each redundancy driver of the bank of memory, the redundancy driver selecting a redundancy driver to activate in response to receiving a selection signal indicative of the memory block in which a memory location corresponding to the memory address is located.

9. The redundancy address decoder of claim 8 wherein the redundancy driver comprises logic circuitry to block the switching of the logic states of the memory address signals applied to the respective redundancy comparison logic when deactivated and to allow the switching of logic states of the memory address signals applied to the respective redundancy comparison logic when activated.

10. The redundancy address decoder of claim 8 wherein the programmable element block comprises a plurality of antifuse elements programmed with column addresses of memory locations mapped to the respective redundancy plane.

11. The redundancy address decoder of claim 10 wherein the selection signals comprise a portion of a row address.

12. The redundancy address decoder of claim 8 wherein the redundancy driver select logic comprises a plurality of NOR gates, each NOR gate having a different combination of the selection signal and its complement as input signals.

13. The redundancy address decoder of claim 8 wherein the redundancy driver comprises a plurality of NAND gates, each NAND gate having a first input coupled to the redundancy driver select logic and a second input to a respective of the input address terminals.

14. A redundancy address decoder, comprising:

a plurality of redundancy comparison circuitry having address terminals at which column addresses are applied and further having an activation terminal for receiving an activation signal, each of the redundancy comparison circuitry coupled to a respective one of the antifuse blocks to compare the column addresses to the programmed addresses in response to receiving an activation signal and to generate a match signal when the column addresses match one of the programmed addresses; and

redundancy comparison selection circuit coupled to each of the redundancy comparison circuitry and having a control signal terminal to which at least one row address signal is applied, the redundancy comparison selection circuit generating an activation signal for activating one of the redundancy comparison circuitry in accordance with the row address signal.

15. The redundancy address decoder of claim 14 wherein the column addresses are represented by a plurality of column address signals and each of the redundancy comparison circuitry comprises:

a redundancy driver having input address terminals to which the column address signals are applied, output address terminals at which output column address signals are

provided, and an activation terminal to which the activation signal from the redundancy comparison selection circuit is applied, the redundancy driver coupling the input address terminals to the output address terminals in response to the activation signal; and

redundancy comparison logic coupled to the respective programmable element block and further coupled to the output address terminals of the redundancy driver to receive the column address signals for comparison to the programmed addresses of the respective programmable element block.

16. The redundancy address decoder of claim 15 wherein the redundancy driver comprises logic circuitry to block the switching of the logic states of the column address signals applied to the respective redundancy comparison logic when deactivated and to allow the switching of logic states of the column address signals applied to the respective redundancy comparison logic when activated.

17. The redundancy address decoder of claim 15 wherein the redundancy driver comprises a plurality of NAND gates, each NAND gate having a first input coupled to the redundancy driver select logic and a second input to a respective one of the input address terminals.

18. The redundancy address decoder of claim 14 wherein the programmable element block comprises a plurality of antifuse elements programmed with column addresses of memory locations mapped to the respective redundancy plane.

19. The redundancy address decoder of claim 14 wherein the redundancy driver select logic comprises a plurality of NOR gates, each NOR gate having a different combination of the row address signal and its complement as input signals.

20. A memory device, comprising:

an address bus to which row and column address signals are provided;

a control bus;

a data bus;

a column address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array divided into at least one bank of memory, each bank of memory segmented into a plurality of memory blocks, each memory block having a respective redundancy plane and a programmable element block storing programmed addresses that are mapped to redundancy memory of the redundancy plane; and

a redundancy address decoder, comprising:

a plurality of redundancy comparison circuitry coupled to a respective one of the programmable element blocks to generate a match signal provided to the column address decoder in response to detecting an address match; and

redundancy driver select logic coupled to each of the redundancy comparison circuitry to activate a selected one of the redundancy comparison circuitry for comparing a portion of a memory address corresponding to a memory location with the programmed addresses of the respective programmable element blocks, the activation by the redundancy driver based on the memory block in which the memory location is located.

21. The memory device of claim 20 wherein the memory address is represented by a plurality of memory address signals provided on the address bus and the redundancy comparison circuitry of the redundancy address decoder comprises:

a redundancy driver having input address terminals to which the memory address signals are applied, output address terminals at which output address signals are provided, and an activation terminal to which an activation signal from the redundancy driver select logic is

applied, the redundancy driver coupling the input address terminals to the output address terminals in response to the activation signal; and

redundancy comparison logic coupled to the respective programmable element block and further coupled to the output address terminals of the redundancy driver to receive the memory address signals for comparison to the programmed addresses of the respective programmable element block.

22. The memory device of claim 21 wherein the redundancy driver of the redundancy address decoder comprises logic circuitry to block the switching of the logic states of the memory address signals applied to the respective redundancy comparison logic when deactivated and to allow the switching of logic states of the memory address signals applied to the respective redundancy comparison logic when activated.

23. The memory device of claim 21 wherein the redundancy driver of the redundancy address decoder comprises a plurality of NAND gates, each NAND gate having a first input coupled to the redundancy driver select logic and a second input to a respective one of the input address terminals.

24. The memory device of claim 20 wherein the programmable element block comprises a plurality of antifuse elements programmed with column addresses of memory locations mapped to the respective redundancy plane.

25. The memory device of claim 20 wherein the redundancy driver select logic of the redundancy address decoder comprises a plurality of NOR gates, each NOR gate having a different combination of a selection signal and its complement as input signals, the selection signal indicative of the memory bank in which the memory location is located.

26. The memory device of claim 25 wherein the portion of the memory address compared by a selected one of the redundancy comparison circuitry comprises a column address and the selection signal comprises a portion of a row address.

27. A memory device, comprising:

an address bus to which row and column address signals are provided;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array divided into at least one bank of memory, each bank of memory segmented into a plurality of memory blocks having a respective redundancy plane of redundant memory; and

a redundancy address decoder, comprising:

for each redundancy plane in a bank of memory, a programmable element block, redundancy comparison logic coupled to the programmable element block, and a redundancy driver coupled to the redundancy comparison logic, the redundancy driver having input address terminals coupled to the address bus to receive memory address signals corresponding to a memory address and having output address terminals to which the memory address signals are coupled in response to activation of the redundancy driver, the comparison logic comparing the memory address signals from the redundancy driver to redundancy memory addresses stored in the programmable element block and generating a match signal provided to the address decoder in response to detecting an address match between the memory address signals and a redundancy memory address; and

redundancy driver select logic coupled to each redundancy driver of the bank of memory, the redundancy driver selecting a redundancy driver to activate in response to

receiving a selection signal indicative of the memory block in which a memory location corresponding to the memory address is located.

28. The memory device of claim 27 wherein the redundancy driver of the redundancy address decoder comprises logic circuitry to block the switching of the logic states of the memory address signals applied to the respective redundancy comparison logic when deactivated and to allow the switching of logic states of the memory address signals applied to the respective redundancy comparison logic when activated.

29. The memory device of claim 27 wherein the programmable element block comprises a plurality of antifuse elements programmed with column addresses of memory locations mapped to the respective redundancy plane.

30. The memory device of claim 29 wherein the selection signals comprise a portion of a row address applied to the address bus.

31. The memory device of claim 27 wherein the redundancy driver select logic of the redundancy address decoder comprises a plurality of NOR gates, each NOR gate having a different combination of the selection signal and its complement as input signals.

32. The memory device of claim 27 wherein the redundancy driver of the redundancy address decoder comprises a plurality of NAND gates, each NAND gate having a first input coupled to the redundancy driver select logic and a second input to a respective of the input address terminals.

33. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus to which row and column address signals are provided;

a control bus;

a data bus;

a column address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array divided into at least one bank of memory, each bank of memory segmented into a plurality of memory blocks, each memory block having a respective redundancy plane and a programmable element block storing programmed addresses that are mapped to redundancy memory of the redundancy plane; and

a redundancy address decoder, comprising:

a plurality of redundancy comparison circuitry coupled to a respective one of the programmable element blocks to generate a match signal provided to the column address decoder in response to detecting an address match; and

redundancy driver select logic coupled to each of the redundancy comparison circuitry to activate a selected one of the redundancy comparison circuitry for comparing a portion of a memory address corresponding to a memory location with the programmed addresses of the respective programmable element blocks, the activation by the redundancy driver based on the memory block in which the memory location is located.

34. The computer system of claim 33 wherein the memory address is represented by a plurality of memory address signals provided on the address bus of the memory device and the redundancy comparison circuitry of the redundancy address decoder comprises:

a redundancy driver having input address terminals to which the memory address signals are applied, output address terminals at which output address signals are provided, and an

activation terminal to which an activation signal from the redundancy driver select logic is applied, the redundancy driver coupling the input address terminals to the output address terminals in response to the activation signal; and

redundancy comparison logic coupled to the respective programmable element block and further coupled to the output address terminals of the redundancy driver to receive the memory address signals for comparison to the programmed addresses of the respective programmable element block.

35. The computer system of claim 34 wherein the redundancy driver of the redundancy address decoder comprises logic circuitry to block the switching of the logic states of the memory address signals applied to the respective redundancy comparison logic when deactivated and to allow the switching of logic states of the memory address signals applied to the respective redundancy comparison logic when activated.

36. The computer system of claim 34 wherein the redundancy driver of the redundancy address decoder comprises a plurality of NAND gates, each NAND gate having a first input coupled to the redundancy driver select logic and a second input to a respective one of the input address terminals.

37. The computer system of claim 33 wherein the programmable element block comprises a plurality of antifuse elements programmed with column addresses of memory locations mapped to the respective redundancy plane.

38. The computer system of claim 33 wherein the redundancy driver select logic of the redundancy address decoder comprises a plurality of NOR gates, each NOR gate having a different combination of a selection signal and its complement as input signals, the selection signal indicative of the memory bank in which the memory location is located.

39. The computer system of claim 38 wherein the portion of the memory address compared by a selected one of the redundancy comparison circuitry comprises a column address and the selection signal comprises a portion of a row address.

40. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus to which row and column address signals are provided;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array divided into at least one bank of memory, each bank of memory segmented into a plurality of memory blocks having a respective redundancy plane of redundant memory; and

a redundancy address decoder, comprising:

for each redundancy plane in a bank of memory, a programmable element block, redundancy comparison logic coupled to the programmable element block, and a redundancy driver coupled to the redundancy comparison logic, the redundancy driver having input address terminals coupled to the address bus to receive memory address signals corresponding to a memory address and having output address terminals to which the memory address signals are coupled in response to activation of the redundancy driver, the comparison logic comparing the memory address signals from the redundancy driver to redundancy memory addresses stored in the programmable element block and generating a match signal provided to

the address decoder in response to detecting an address match between the memory address signals and a redundancy memory address; and

redundancy driver select logic coupled to each redundancy driver of the bank of memory, the redundancy driver selecting a redundancy driver to activate in response to receiving a selection signal indicative of the memory block in which a memory location corresponding to the memory address is located.

41. The computer system of claim 40 wherein the redundancy driver of the redundancy address decoder comprises logic circuitry to block the switching of the logic states of the memory address signals applied to the respective redundancy comparison logic when deactivated and to allow the switching of logic states of the memory address signals applied to the respective redundancy comparison logic when activated.

42. The computer system of claim 40 wherein the programmable element block comprises a plurality of antifuse elements programmed with column addresses of memory locations mapped to the respective redundancy plane.

43. The computer system of claim 42 wherein the selection signals comprise a portion of a row address applied to the address bus.

44. The computer system of claim 40 wherein the redundancy driver select logic of the redundancy address decoder comprises a plurality of NOR gates, each NOR gate having a different combination of the selection signal and its complement as input signals.

45. The computer system of claim 40 wherein the redundancy driver of the redundancy address decoder comprises a plurality of NAND gates, each NAND gate having a first input coupled to the redundancy driver select logic and a second input to a respective of the input address terminals.

46. A method of comparing a memory address represented by memory address signals to programmed addresses stored in a plurality of programmable element blocks, each programmable element block identifying memory locations in a respective memory block to be mapped to a respective redundancy plane, the method comprising:

gating the memory address for comparison with the programmed addresses of the programmable element block identifying the memory locations of the memory block in which the memory location corresponding to the memory address is located;

blocking the memory address from comparison with the programmed addresses of the programmable element blocks for non-selected redundancy planes; and

generating a match signal in response to the memory address matching one of the programmed addresses of the programmable element block to which the memory address is gated.

47. The method of claim 46 wherein gating the memory address for comparison comprises:

providing the memory address signals to a respective set of logic gates, one set for each of the redundancy planes; and

generating an activation signal provided to the set of the logic gates of the redundancy plane for the memory block in which the memory location corresponding to the address signals is located to provide output signals from the set logic gates representative of the memory address signals.

48. The method of claim 47 wherein blocking the memory address from comparison comprises generating activation signals provided to the sets of logic gates for the remaining redundancy planes to generate output signals from the sets of logic gates having constant logic levels.

49. The method of claim 46 wherein the memory address is represented by row and column address signals, and the method further comprises:

evaluating a portion of the row address signals; and

based on the address signals, identifying the memory block in which the memory location corresponding to the memory address is located.

50. The method of claim 46 wherein gating the memory address and blocking the memory address comprises gating and blocking column address signals.

51. A method of determining mapping of memory locations corresponding to row and column memory addresses in a bank of memory segmented into memory blocks having a respective redundancy plane and antifuse block, the antifuse block storing programmed address of memory locations in the respective memory block mapped to the respective redundancy plane, the method comprising:

evaluating a portion of the row memory address to identify in which of the memory blocks the memory location is located; and

comparing the column address to the programmed addresses of only the antifuse block of the redundancy plane for the memory block in which the memory location is located.

52. The method of claim 51 wherein comparing the column address to the programmed addresses of only the antifuse block comprises:

gating the column address signals for comparison with the programmed addresses of the programmable element block identifying the memory locations of the memory block in which the memory location corresponding to the memory address is located; and

blocking the column address signals from comparison with the programmed addresses of the programmable element blocks for the remaining redundancy planes.

53. The method of claim 52 wherein gating the column address signals for comparison comprises:

providing the column address signals to a respective set of logic gates, one set for each of the redundancy planes; and

generating an activation signal provided to the set of the logic gates of the redundancy plane for the memory block in which the memory location corresponding to the address signals is located to provide output signals from the set logic gates representative of the column address signals.

54. The method of claim 52 wherein blocking the column address signals from comparison comprises generating activation signals provided to the sets of logic gates for the remaining redundancy planes to generate output signals from the sets of logic gates having constant logic levels.